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EXAMINER
TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/976,708	DORSEY, MICHAEL C.
	Examiner	Art Unit
	John P Trimmings	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _12 October 2001_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-33_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-33_ is/are rejected.

7)☒ Claim(s) _24, 25 and 31_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _12 October 2001_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claims 1-33 are presented for examination.

Information Disclosure Statement

The examiner has considered the applicant's Disclosure Statements of

3/27/2003.

Drawings

1.   The drawings are objected to because:

    a.   FIG.1 logic components 195 are referenced as 195a-d in the disclosure.

    b.   FIG.2 LSSD and STEP CLKS are not referred to in the disclosure.

    c.   FIG.9 LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and

        LBST_SDCAN_CLKB are not referred to in the disclosure.

A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not

be held in abeyance.

Specification

2.   The disclosure is objected to because of the following informalities: page 7 line 8

describes engine 110 being configured by a 66 bit signal composed of a 32 bit vector

and 33 bit seed. The sum of 32 and 33 is not 66. Appropriate correction is required.

3.   The disclosure is objected to because of the following informalities: page 9 line 24 recites, "(bits B_{26} to B_0)", but the examiner believes that it should read, "(bits B_{30} to B_0)". Appropriate correction is required.

4.   The disclosure is objected to because of the following informalities: page 9 line 34 recites, "LBST_STEP_STEPE", but the examiner cannot find this reference in FIG.9. Appropriate correction is required.

5.   The disclosure is objected to because of the following informalities: page 10 line 8 recites, "components 150", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

6.   The disclosure is objected to because of the following informalities: page 13 lines 28 and 30 recite, "ASIC 100", but the examiner cannot find this reference in the drawings, and believes it should read "ASIC 150". Appropriate correction is required.

7.   The disclosure is objected to because of the following informalities: page 13 line 31 recites, "925 including", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

8.   The disclosure is objected to because of the following informalities: page 14 line 8 recites, "controller 925", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

Claim Objections

9.   Claims 24, 25 and 31 are objected to because of the following informalities: in

order to achieve a clearer understanding of the claim, the examiner suggests dropping

the word "is" in each claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

10.   Claims 23 and 30 recite the limitation "the first primitive polynomial" in line 1 and

2. There is insufficient antecedent basis for this limitation in the claim.

11.   Claim 26 recites the limitation "the dual mode built-in self-test controller" in line 4.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

   1.   Determining the scope and contents of the prior art.
   2.   Ascertaining the differences between the prior art and the claims at issue.

3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
obviousness or nonobviousness.

12.   Claims 1, 3, 5, 8, 10, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being

unpatentable over McNamara et al., U.S. Patent No. 6629281, and in view of Heon-

Cheol Kim, U.S. Patent No. 5938784.

As per Claim 1, 5, 8 and 22:

McNamara et al. teaches a BIST method and controller (see Abstract and

column 1 lines33-44) comprising a LBIST engine (column 3 lines 27-31) and means for

executing a LBIST (column 4 lines 27-28 and line 43), including an LBIST state machine

(column 1 lines 44-48). McNamara et al. also teaches a pattern generator (column 1

lines 60-61) and storing compressed signature results (column 1 lines 60-67) but fails to

teach the pattern generator as being based on a 1st primitive polynomial, and the

signature register to be a MISR, based on a 2nd primitive polynomial. In an analogous

art, Kim teaches prior art and the Kim invention as having an LFSR (pattern generator)

and a MISR, both being based on primitive polynomials (see Abstract, column 1 lines

33-59 and column 2 lines 1-6 and column s lines 20-67 and column 4 lines 1-28). And

Kim, in column 1 lines 60-67 and column 2 lines 1-9 states that the invention reduces

the number of dedicated logic for the BIST controller. One with ordinary skill in the art at

the time of the invention, motivated as suggested by Kim, would combine the two

references, and so the claims are rejected.

As per Claims 3, 10, 24 and 25:

Dependent on Claims 1 or 8 or 22, the claims limit the 2nd primitive polynomial to

$x^{32} + x^{28} + x + 1$. The primitive polynomials available to the user in Kim, due to the broad

scope, includes this polynomial by default, and in view of the previous motivation in

Claims 1, 8 and 22, the claims are rejected.

13.   Claims 2, 9 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable

over McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S.

Patent No. 5938784 as applied to Claims 1 or 22, and further in view of Paul H. Bardell

Jr., U.S. Patent No. 4959832. Dependent on Claims 1 or 8 or 22, the claims limit the 1st

primitive polynomial to $x^{31} + x^3 + 1$. In an analogous art, Bardell Jr. teaches this specific

primitive polynomial in column 8 line 36. And Bardell Jr., in column 2 lines 29-67 recites

the advantage of increased effectiveness in BIST by using the subject phase shift

enhancement. One with ordinary skill in the art at the time of the invention, motivated to

better BIST effectiveness as suggested, would combine the references, and so the

claims are rejected.

14.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784 as applied to Claim 1 above, and further in view of of Simpson et al., U.S.

Patent No. 5260950, Wong et al., U.S. Patent No. 6636997, and Bogholtz et al., U.S.

Patent No. 5357523. The LBIST state machine in Claim 1 is further limited to a reset

state entered via an external signal. Simpson et al. enters a reset state (column 1 lines

24-36) via an external reset signal (Drawing, RESET 11), but does not begin initializing

the device with an LBIST run signal. And Simpson et al., in column 1 lines 5-9 states the

advantage of being able to provide a reset signal the circuit under test to a safe state. In

McNamara et al. the device enters an initiate state subsequent to a start ABIST signal

(column 2 lines 55-67), and suggests a similar LBIST in the same invention (column 3

lines 27-32). An analogous art, Wong et al. in column 6 lines 26-50 teaches the states

of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in

column 2 lines 62-67, describes an advantage of the invention as being capable of both

pseudo-random and functional testing, but does not complete the test by comparing the

pattern generator to a counter set-point. Lastly, an analogous art, Bogholtz et al.,

teaches ending the BIST under the condition of comparing the pattern generator to a

pre-set count (FIG.10 32 and column 8 lines 27-40), and column 2 lines 7-10 specify an

advantage as being a way to flexibly configure the test parameters. And in view of the

motivations stated within this paragraph, one with ordinary skill in the art at the time of

the invention would combine all of the references above, and thus the claim is rejected.

15.   Claims 7, 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable

over McNamara et al., U.S. Patent No. 6629281, and in view of Heon-Cheol Kim, U.S.

Patent No. 5938784 as applied to Claims 1 or 8 or 22 above, and in view of Rajski et al.,

U.S. Patent No. 5991909. Dependent on Claims 1 or 8 or 22 above, the claims limit the

seeding of the pattern generator to being externally configurable. In an analogous art,

Rajski et al. sets the LFSR (column 7 lines 15-23) to an external seed (FIG.3 108) via

an input port. And Rajski et al., in column 3 lines 31-34 recites the advantage of testing

with variable reseeding that is compatible with JTAG protocols. One with ordinary skill in

the art at the time of the invention, motivated by Rajski et al. as indicated, would

combine the references, and so the claims are rejected.

16.   Claims 6, 12, 14, 16, 17, 18 and 27 are rejected under 35 U.S.C. 103(a) as being

unpatentable over McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol

Kim, U.S. Patent No. 5938784, and further in view of Motika et al., U.S. Patent No.

5982189.

As per Claims 6, 17 and 27:

Dependent on Claims 1 or 12 or 22, the claims further limit the controller wherein the

signature register includes a bit indicating the LBIST is done. Motika et al., in column 3

lines 39-67 and column 4 lines 1-5 teaches a LBIST where the signature includes a

pass/fail indicator. A pass/fail indicator is the same as a test done indicator – the testing

must be done if there is a pass/fail indication. And column 1 lines 65-67 specifies of

Motika et al. recites an advantage to be a better stress test for circuits. One with

ordinary skill in the art at the time of the invention, motivated by Motika et al., would

combine the references, and so the claims are rejected.

As per Claim 12, 16 and 18:

McNamara et al. teaches a BIST controller (see Abstract and column 1 lines33-

44) comprising a LBIST or MBIST engine (column 3 lines 27-31) and means for

executing a LBIST or MBIST (column 4 lines 27-28 and line 43), including an LBIST or

MBIST state machine (column 1 lines 44-48). McNamara et al. also teaches a pattern

generator (column 1 lines 60-61) and storing compressed signature results (column 1

lines 60-67) but fails to teach the pattern generator as being based on a 1st primitive

polynomial, and the signature register to be a MISR, based on a 2nd primitive

polynomial. In an analogous art, Kim teaches prior art and the Kim invention as having

an LFSR (pattern generator) and a MISR, both being based on primitive polynomials

(see Abstract, column 1 lines 33-59 and column 2 lines 1-6 and column s lines 20-67

and column 4 lines 1-28). And Kim, in column 1 lines 60-67 and column 2 lines 1-9

states that the invention reduces the number of dedicated logic for the BIST controller.

However, the references fail to teach a plurality of memory components, a logic core,

and a testing interface. In an analogous art, Motika et al. teaches these features in

FIG.2 as memories (FIG.2 36), a logic core (FIG.2 38), and tester interface (FIG.2 60).

One with ordinary skill in the art at the time of the invention, motivated as suggested by

Kim above and Motika et al. elsewhere in this office action would combine the

references, and so the claims are rejected.

As per Claim 14:

Dependent on Claim 12, the claim limits the 2nd primitive polynomial to $x^{32} + x^{28} + x + 1$. The primitive polynomials available to the user in Kim, due to the broad scope,

includes this polynomial by default, and in view of the previous motivation in Claim 12,

the claim is rejected.

17.   Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784, and further in view of Motika et al., U.S. Patent No. 5982189 as applied to

Claim 12, and further in view of Paul H. Bardell Jr., U.S. Patent No. 4959832.

Dependent on Claim 12, the claim limits the 1st primitive polynomial to $x^{31} + x^3 + 1$. In

an analogous art, Bardell Jr. teaches this specific primitive polynomial in column 8 line

36. And Bardell Jr., in column 2 lines 29-67 recites the advantage of increased

effectiveness in BIST by using the subject phase shift enhancement. One with ordinary

skill in the art at the time of the invention, motivated to better BIST effectiveness as

suggested, would combine the references, and so the claim is rejected.

18.   Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784, and further in view of Motika et al., U.S. Patent No. 5982189 as applied to

Claim 12 above, and further in view of of Simpson et al., U.S. Patent No. 5260950,

Wong et al., U.S. Patent No. 6636997, and Bogholtz et al., U.S. Patent No. 5357523.

The LBIST state machine in Claim 12 is further limited to a reset state entered via an

external signal. Simpson et al. enters a reset state (column 1 lines 24-36) via an

external reset signal (Drawing, RESET 11), but does not begin initializing the device

with an LBIST run signal. And Simpson et al., in column 1 lines 5-9 states the

advantage of being able to provide a reset signal the circuit under test to a safe state. In

McNamara et al. the device enters an initiate state subsequent to a start ABIST signal

(column 2 lines 55-67), and suggests a similar LBIST in the same invention (column 3

lines 27-32). An analogous art, Wong et al. in column 6 lines 26-50 teaches the states

of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in

column 2 lines 62-67, describes an advantage of the invention as being capable of both

pseudo-random and functional testing, but does not complete the test by comparing the

pattern generator to a counter set-point. Lastly, an analogous art, Bogholtz et al.,

teaches ending the BIST under the condition of comparing the pattern generator to a

pre-set count (FIG.10 32 and column 8 lines 27-40), and column 2 lines 7-10 specify an

advantage as being a way to flexibly configure the test parameters. And in view of the

motivations stated within this paragraph, one with ordinary skill in the art at the time of

the invention would combine all of the references above, and thus the claim is rejected.

19.   Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 12

above, and further in view of Kim et al., U.S. Patent No. 6148426. Dependent on Claim

12, this claim limits a memory device to being a static random access memory. In an

analogous art, Kim et al. teaches an MBIST (see Abstract) that is used for testing an

SRAM (see Title). Citing a savings in BIST size and cost (column 2 lines 55-61), Kim et

al. would motivate one with ordinary skill in the art at the time of the invention to

combine the art for the purpose of testing SRAM memories.

20.   Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 12

above, and further in view of Au et al., U.S. Patent No. 6681359. Dependent on Claim

12, this claim limits a test interface to a JTAG TAP Controller. In Au et al., FIG.3 112 is

a JTAG TAP Controller, and Au et al., in column 2 lines 18-27 in reciting the attributes of

the invention, boasts of a better means to retrieve information within an MBIST while not

requiring a large number of device pins. One with ordinary skill in the art at the time of

the invention, motivated by Au et al., would combine the two references, thus the claims

are rejected.

21.   Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784, and in view of Motika et al., U.S. Patent No. 5982189 as applied to Claim 12

above, and further in view of Rajski et al., U.S. Patent No. 5991909. Dependent on

Claim 12 above, the claim limits the seeding of the pattern generator to being externally

configurable. In an analogous art, Rajski et al. sets the LFSR (column 7 lines 15-23) to

an external seed (FIG.3 108) via an input port. And Rajski et al., in column 3 lines 31-34

recites the advantage of testing with variable reseeding that is compatible with JTAG

protocols. One with ordinary skill in the art at the time of the invention, motivated by

Rajski et al. as indicated, would combine the references, and so the claims are rejected.

22.   Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over

McNamara et al., U.S. Patent No. 6629281, in view of Heon-Cheol Kim, U.S. Patent No.

5938784, as applied to Claim 22 above, and further in view of Wong et al., U.S. Patent

No. 6636997, and Bogholtz et al., U.S. Patent No. 5357523. The LBIST method of

Claim 22 is further defined whereas it initializes the device with an LBIST run signal. In

McNamara et al. the device enters an initiate state subsequent to a start ABIST signal

(column 2 lines 55-67), and suggests a similar LBIST in the same invention (column 3

lines 27-32). An analogous art, Wong et al. in column 6 lines 26-50 teaches the states

of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in

column 2 lines 62-67, describes an advantage of the invention as being capable of both

pseudo-random and functional testing, but does not complete the test by comparing the

pattern generator to a counter set-point. Lastly, an analogous art, Bogholtz et al.,

teaches ending the BIST under the condition of comparing the pattern generator to a

pre-set count (FIG.10 32 and column 8 lines 27-40), and column 2 lines 7-10 specify an

advantage as being a way to flexibly configure the test parameters. And in view of the

motivations stated within this paragraph, one with ordinary skill in the art at the time of

the invention would combine all of the references above, and thus the claim is rejected.

23.   Claims 29, 31, 32 and 33 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Au et al., U.S. Patent No. 6681359, in view of Rajski et al., U.S.

Patent No. 5991909, in view of Heon-Cheol Kim, U.S. Patent No. 5938784.

As for Claim 29:

Au et al. teaches a method for testing an integrated circuit device (see Abstract),

the method comprising: interfacing the integrated circuit device with a tester (column 8

lines 29-31); performing a built-in self-test (column 8 lines 56-58), and reading the

indication (column 10 lines 21-26). Au et al. however fails to teach, seeding a pattern

generator with a 1st polynomial, performing a LBIST and storing results in a MISR using

a 2nd primitive polynomial. In an analogous art, Rajski et al. does teach seeding a

pattern generator (FIG.3 106 and column 3 lines 59-62 and column 7 line 18) with any

polynomial (column 8 line 64), performing a LBIST (column 1 lines 5-10), and storing

results in a MISR (FIG.1 28), but does not teach using a primitive polynomial in the

MISR. But Kim does teach using a primitive polynomial (see Kim Absract). And in view

of the motivation previously set forth for Rajski et al. and Kim, one with ordinary skill in

the art at the time of the invention would combine the references, and so the claim is

rejected.

As per Claim 31:

Dependent on Claim 29, the claim limits the 2nd primitive polynomial to $x^{32} + x^{28} +$

$x + 1$. The primitive polynomials available to the user in Kim, due to the broad scope,

includes this polynomial by default, and in view of the previous motivation in Claims 29,

the claim is rejected.

As per Claim 32:

The method of Claim 29 is limited to externally configuring the seed. Rajski et al.,

in FIG3 108 describes the same feature, and in view of the previous motivation, the

claim is rejected.

As per Claim 33:

The method of Claim 29 is further limited to performing a MBIST. Au et al.,

describes this feature in the Abstract, and in view of the motivation previously

mentioned, the claim is rejected.

24.   Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al.,

U.S. Patent No. 6681359, in view of Rajski et al., U.S. Patent No. 5991909, and in view

of Heon-Cheol Kim, U.S. Patent No. 5938784 as applied to Claim 29, and further in

view of Paul H. Bardell Jr., U.S. Patent No. 4959832. Dependent on Claim 29, the claim

limits the 1st primitive polynomial to $x^{31} + x^3 + 1$. In an analogous art, Bardell Jr. teaches

this specific primitive polynomial in column 8 line 36. And Bardell Jr., in column 2 lines

29-67 recites the advantage of increased effectiveness in BIST by using the subject

phase shift enhancement. One with ordinary skill in the art at the time of the invention,

motivated to better BIST effectiveness as suggested, would combine the references,

and so the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to John P Trimmings whose telephone number is 703-305-

0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Albert DeCady
Primary Examiner